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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/675,525	09/29/2003	John Bruno	00100.03.0034	6091

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EXAMINER	
SUGENT, JAMES F	
ART UNIT	**PAPER NUMBER**
2116	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	12/20/2006	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/675,525	BRUNO ET AL.	
	Examiner	Art Unit	
	James F. Sugent	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 October 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *12,13,15-19 and 34-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *10/26/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is sent in response to Applicant's Communication received October 30, 2006 for application number 10/675,525 originally filed September 29, 2003. The Office hereby acknowledges receipt of the following and placed of record in file: Request for Continued Examination and amended claims 1-36 wherein claims 1-11, 14 and 20-33 have been canceled and claims 34-36 are new.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 12, 13, 15 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Meynard (U.S. Patent Publication No. 2003/0229816 A1) (hereinafter referred to as Meynard) in view of Mahalingaiah et al. (U.S. Patent No. 5,490,059) (hereinafter referred to as Mahalingaiah).

As to claim 12, Meynard discloses a clock control system for generating a clock signal having an operating frequency set to a nominal operating frequency corresponding to a maximum rated junction temperature, comprising: a thermal sensor (280 or 520) operative to produce a temperature signal corresponding to a junction temperature of at least a portion of a circuit on a die (paragraphs 53, 64 and 72); a clock generator circuit (270) operative to produce the clock signal (paragraphs 53 and 54); and a dynamic overclock frequency control data generator (230 or 530), operatively coupled to the clock generator circuit (as shown in Fig. 2), and operative to provide dynamic overclock frequency control data (via 231 or 550) to the clock generator circuit in response to the control signal and the received temperature signal to cause the clock generator circuit to increase the operating frequency of the clock signal above the nominal operating frequency, when the detected junction temperature is less than a temperature threshold (paragraphs 38, 53-56, 62-64 and 72-78).

Meynard does not explicitly disclose a thermal sensor control circuit, operatively coupled to the thermal sensor, and operative to produce temperature data in response to the temperature signal and to provide a control signal in response to the temperature data; or, that the temperature threshold is the maximum rated junction temperature.

Mahalingaiah teaches a clock controlling system that dynamically responds to temperature readings on the die of a processing chip (Abstract). Mahalingaiah further teaches a

thermal sensor control circuit (134) that receives the sensed temperature from the sensor (130) and creates temperature data (control [1:0]) that is sent to a clock control generator (110) (column 3, lines 41-57). Mahalingaiah further teaches temperature threshold used to determine safe operating conditions is based on the maximum rated junction temperature (maximum threshold temperature) (column 1, lines 23-28 and column 6, lines 14-35). Mahalingaiah has the additional feature of controlling the system clock which is temperature dependent in addition to the processor clock (column 2, lines 2-7).

It would have been obvious to one of ordinary skill of the art having the teachings of Meynard and Mahalingaiah at the time the invention was made, to modify clock control system of Meynard to include the thermal sensor control circuit and the temperature threshold of the maximum rated junction temperature as taught by Mahalingaiah. One of ordinary skill in the art would be motivated to make this combination of including the thermal sensor control circuit and the temperature threshold of the maximum rated junction temperature in view of the teachings of Mahalingaiah, as doing so would give the added benefit of controlling the system clock which is temperature dependent in addition to the processor clock (as taught by Mahalingaiah above).

As to claims 13, 15 and 16, they are directed to the clock control system of steps set forth in claim 12. Therefore, they are rejected for the same basis as set forth hereinabove.

Claims 17-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Williams et al. (U.S. Patent No. 6,397,343 B1) (hereinafter referred to as Williams) in view of Mahalingaiah (as cited above).

As to claim 17, Williams discloses in a system comprising a host processor and a graphics co-processor, a method for generating a clock signal for the graphics co-processor, the clock signal having an operating frequency set to a nominal operating frequency corresponding to a maximum rated junction temperature (Abstract), the method comprising: detecting, by a thermal sensor (302) coupled to the graphics co-processor, a junction temperature corresponding to at least a portion of a circuit on a die constituting at least a portion of the graphics co-processor, thereby providing a temperature signal (column 9, lines 9-26 and column 9, lines 47-63); and causing, by the host processor in response to the temperature signal, an increase in the operating frequency of the clock signal above the nominal operating frequency, when the detected temperature is less than a temperature threshold (Abstract and column 4, lines 12-47 and column 9, lines 9-63 and column 10, lines 16-32 and column 10, lines 40-48 and column 12, lines 30-52).

Williams does not explicitly disclose a thermal sensor control circuit, operatively coupled to the thermal sensor, and operative to produce temperature data in response to the temperature signal and to provide a control signal in response to the temperature data; or, that the temperature threshold is the maximum rated junction temperature.

Mahalingaiah teaches a clock controlling system that dynamically responds to temperature readings on the die of a processing chip (Abstract). Mahalingaiah further teaches a thermal sensor control circuit (134) that receives the sensed temperature from the sensor (130) and creates temperature data (control [1:0]) that is sent to a clock control generator (110) (column 3, lines 41-57). Mahalingaiah further teaches temperature threshold used to determine safe operating conditions is based on the maximum rated junction temperature (maximum

threshold temperature) (column 1, lines 23-28 and column 6, lines 14-35). Mahalingaiah has the additional feature of controlling the system clock which is temperature dependent in addition to the processor clock (column 2, lines 2-7).

It would have been obvious to one of ordinary skill of the art having the teachings of Williams and Mahalingaiah at the time the invention was made, to modify the clock control method of Williams to include the thermal sensor control circuit and the temperature threshold of the maximum rated junction temperature as taught by Mahalingaiah. One of ordinary skill in the art would be motivated to make this combination of including the thermal sensor control circuit and the temperature threshold of the maximum rated junction temperature in view of the teachings of Mahalingaiah, as doing so would give the added benefit of controlling the system clock which is temperature dependent in addition to the processor clock (as taught by Mahalingaiah above).

As to claims 18 and 19, they are directed to the clock control method of steps set forth in claim 17. Therefore, they are rejected for the same basis as set forth hereinabove.

Claims 34-36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Meynard (as cited above) in view of Mahalingaiah (as cited above) and in further view of Helms et al. (U.S. Patent Publication No. 2003/0110423 A1) (hereinafter referred to as Helms) (cited by Applicant).

As to claim 34, Meynard discloses a clock control system for generating a clock signal having an operating frequency set to a nominal operating frequency corresponding to a

maximum rated junction temperature, comprising: a thermal sensor (280 or 520) operative to produce a temperature signal corresponding to a junction temperature of at least a portion of a circuit on a die (paragraphs 53, 64 and 72); a clock generator circuit (270) operative to produce the clock signal (paragraphs 53 and 54); and a dynamic overclock frequency control data generator (230 or 530), operatively coupled to the clock generator circuit (as shown in Fig. 2), and operative to provide dynamic overclock frequency control data (via 231 or 550) to the clock generator circuit in response to the control signal and the received temperature signal to cause the clock generator circuit to increase the operating frequency of the clock signal above the nominal operating frequency, when the detected junction temperature is less than a temperature threshold (paragraphs 38, 53-56, 62-64 and 72-78).

Meynard does not explicitly disclose a thermal sensor control circuit, operatively coupled to the thermal sensor, and operative to produce temperature data in response to the temperature signal and to provide a control signal in response to the temperature data; or, that the temperature threshold is the maximum rated junction temperature.

Mahalingaiah teaches a clock controlling system that dynamically responds to temperature readings on the die of a processing chip (Abstract). Mahalingaiah further teaches a thermal sensor control circuit (134) that receives the sensed temperature from the sensor (130) and creates temperature data (control [1:0]) that is sent to a clock control generator (110) (column 3, lines 41-57). Mahalingaiah further teaches temperature threshold used to determine safe operating conditions is based on the maximum rated junction temperature (maximum threshold temperature) (column 1, lines 23-28 and column 6, lines 14-35). Mahalingaiah has the

additional feature of controlling the system clock which is temperature dependent in addition to the processor clock (column 2, lines 2-7).

It would have been obvious to one of ordinary skill of the art having the teachings of Meynard and Mahalingaiah at the time the invention was made, to modify clock control system of Meynard to include the thermal sensor control circuit and the temperature threshold of the maximum rated junction temperature as taught by Mahalingaiah. One of ordinary skill in the art would be motivated to make this combination of including the thermal sensor control circuit and the temperature threshold of the maximum rated junction temperature in view of the teachings of Mahalingaiah, as doing so would give the added benefit of controlling the system clock which is temperature dependent in addition to the processor clock (as taught by Mahalingaiah above).

Neither Meynard nor Mahalingaiah explicitly teach a memory comprising data representing a lookup table containing junction temperatures over a temperature operating range with corresponding clock signal frequencies.

Helms teaches a dynamic state performance system also alters the clock speed to a processor dependent on temperature of the processor die (column 6, line 41 thru column 7, line 58). Helms also teaches a memory (BIOS) can store the data representing a lookup table (Fig. 4) containing junction temperatures over a temperature operating range with corresponding clock signal frequencies (column 7, lines 59-64). Helms also teaches more detail of the functions dependent on the measured temperatures (Fig. 5 and column 7, line 65 thru column 8, line 26).

It would have been obvious to one of ordinary skill of the art having the teachings of Meynard, Mahalingaiah and Helms at the time the invention was made, to modify the clock control system of Meynard to include a look-up table in memory as taught by Helms. One of

ordinary skill in the art would be motivated to make this combination of including a look-up table in memory in view of the teachings of Helms, as doing so would give the added benefit of further reducing power consumption by the system.

As to claim 34, Meynard discloses a clock control system for generating a clock signal having an operating frequency set to a nominal operating frequency corresponding to a maximum rated junction temperature, comprising: a thermal sensor (280 or 520) operative to produce a temperature signal corresponding to a junction temperature of at least a portion of a circuit on a die (paragraphs 53, 64 and 72); a clock generator circuit (270) operative to produce the clock signal (paragraphs 53 and 54); and a dynamic overclock frequency control data generator (230 or 530), operatively coupled to the clock generator circuit (as shown in Fig. 2), and operative to provide dynamic overclock frequency control data (via 231 or 550) to the clock generator circuit in response to the control signal and the received temperature signal to cause the clock generator circuit to increase the operating frequency of the clock signal above the nominal operating frequency, when the detected junction temperature is less than a temperature threshold (paragraphs 38, 53-56, 62-64 and 72-78).

Meynard does not explicitly disclose a thermal sensor control circuit, operatively coupled to the thermal sensor, and operative to produce temperature data in response to the temperature signal and to provide a control signal in response to the temperature data; or, that the temperature threshold is the maximum rated junction temperature.

Mahalingaiah teaches a clock controlling system that dynamically responds to temperature readings on the die of a processing chip (Abstract). Mahalingaiah further teaches a thermal sensor control circuit (134) that receives the sensed temperature from the sensor (130)

and creates temperature data (control [1:0]) that is sent to a clock control generator (110) (column 3, lines 41-57). Mahalingaiah further teaches temperature threshold used to determine safe operating conditions is based on the maximum rated junction temperature (maximum threshold temperature) (column 1, lines 23-28 and column 6, lines 14-35). Mahalingaiah has the additional feature of controlling the system clock which is temperature dependent in addition to the processor clock (column 2, lines 2-7).

It would have been obvious to one of ordinary skill of the art having the teachings of Meynard and Mahalingaiah at the time the invention was made, to modify clock control system of Meynard to include the thermal sensor control circuit and the temperature threshold of the maximum rated junction temperature as taught by Mahalingaiah. One of ordinary skill in the art would be motivated to make this combination of including the thermal sensor control circuit and the temperature threshold of the maximum rated junction temperature in view of the teachings of Mahalingaiah, as doing so would give the added benefit of controlling the system clock which is temperature dependent in addition to the processor clock (as taught by Mahalingaiah above).

Neither Meynard nor Mahalingaiah explicitly teach a clock frequency is controlled using interrupts.

Helms teaches a dynamic state performance system also alters the clock speed to a processor dependent on temperature of the processor die (column 6, line 41 thru column 7, line 58). Helms also teaches a memory (BIOS) can store the data representing a lookup table (Fig. 4) containing junction temperatures over a temperature operating range with corresponding clock signal frequencies (column 7, lines 59-64). Helms also teaches more detail of the functions dependent on the measured temperatures (Fig. 5 and column 7, line 65 thru column 8, line 26).

Helms further teaches the temperature threshold crossing control signals are interrupt driven (column 8, lines 56-67).

It would have been obvious to one of ordinary skill of the art having the teachings of Meynard, Mahalingaiah and Helms at the time the invention was made, to modify the clock control system of Meynard to include the control signals are interrupt signals as taught by Helms. One of ordinary skill in the art would be motivated to make this combination of including the control signals are interrupt signals in view of the teachings of Helms, as doing so would give the added benefit of further reducing power consumption by the system.

As to claim 36, it is directed to the clock control system of steps set forth in claim 35. Therefore, it is rejected for the same basis as set forth hereinabove.

Conclusion

Any inquiry concerning this communication or earlier communications from the Examiner should be directed to James Sugent whose telephone number is (571) 272-5726. The Examiner can normally be reached on 8AM - 4PM.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Rehana Perveen can be reached on (571) 272-3676. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished

applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at (866) 217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call (800) 786-9199 (IN USA OR CANADA) or (571) 272-1000.

James F. Sugent
Patent Examiner, Art Unit 2116
December 14, 2006

THUAN N. DU
PRIMARY EXAMINER